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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): SUZUKI et al.	
Application No.: 10/729,955	Group Art Unit: 2815
Filed: December 9, 2003	Examiner: LEE, Eugene
Title: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	
Attorney Docket No.: 01-528	

October 21, 2004

Commissioner for Patents
U.S. Patent and Trademark Office
220 20th Street, South
Customer Window
Crystal Plaza Two, Lobby, Room 1B03
Arlington, VA 22202

RESPONSE TO RESTRICTION REQUIREMENT AND ELECTION OF SPECIES

Sir:

In response to the Election of Species Requirement mailed on September 22, 2004 in connection with the above application, Applicants hereby elect Group I claims (claims 1-14, 16 and 18-25), drawn to a semiconductor device, and Species I of Fig. 2, with traverse.

Regarding the restriction requirement, the Examiner asserts that the product as claimed can be made by another and materially different process, and has indicated that doping can be used instead of ion implantation as recited in claims 15 and 17. However, as indicated in an excerpt from VLSI Fabrication Principles, which is attached as Exhibit A, ion implantation is one technique used for doping. Therefore, the two methods are not materially different processes as asserted by the Examiner.

In addition, because method claims 15 and 17 depend from device claims 1 and 16, respectively, the methods as claimed are specifically for making only the product as recited in claims 1 and 16.

Therefore, as the inventions are not distinct for the reasons given by the Examiner, Applicants respectfully request that the Examiner's restriction requirement be withdrawn, and that claims 1-25 be examined together in the present application.

Regarding the election of species requirement, Applicants state that claims 1, 2, 8, 16, 18 and 19 read on Species I of Fig. 2. Contrary to the Examiner's assertion that no claims are currently generic, Applicants assert that claims 1, 2, 8, 16, 18 and 19 are generic to all species identified by the Examiner (Species I-X).

For example, Species II in Fig. 11A differs from Species I in Fig. 2 only in that, *inter alia*, the depth of the N^+ source region is deeper than that in Species I, thereby enabling current to flow to a deeper portion of the trench 35. (See, for example, page 26, lines 1-12.)

Species III in Fig. 14A differs from Species I in Fig. 2 only in that the surface gate electrode 39 is arranged to extend to an upper position on the side of the source N^+ region 31, and that the gate electrode 37 in the trench is arranged in the opening of the source N^+ region 31 on the side of the trench 35, to increase current flow. (See, for example, page 27, lines 7-14.)

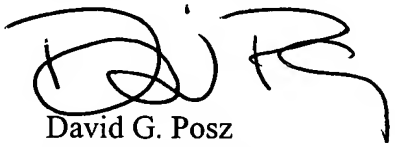
Species IV in Fig. 15 differs from Species I in Fig. 2 only in that the semiconductor device is formed in a manner that prevents impurities used to form the base contact region from diffusing to the trench 35. (See, for example, page 29, lines 1-2.)

Therefore, the aforementioned generic claims read on Species I-IV, as well as Species V-X. If assuming *arguendo* that the Examiner disagrees with the above assertion that claims 1, 2, 8, 16, 18 and 19 are generic to all species identified by the Examiner, Applicants request that the Examiner provide specific reasons as to why he believes that the claims are not generic.

Examination of the present application in view of the above election is respectfully requested.

Please charge any necessary fees to Deposit Account 50-1147.

Respectfully submitted,



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forming the various devices that are required in the circuit. Proton implantation has also been used as an alternative isolation technique [102].

Microcircuits can also be fabricated by direct implantation into SI GaAs substrates. This approach has the advantage that it results in a planar topology, since mesa etching is not necessary to obtain isolation between components. The resulting planar surface greatly simplifies the task of photolithography at the submicron level, and allows fabrication of ultrahigh-speed circuits [103, 104]. Advanced designs, using self-aligned refractory gate technology, have also been developed to exploit the high-speed capabilities of GaAs FETs in integrated circuits [105].

In all of these techniques, the main impetus for using ion implantation is its ability to provide precise control of the doping and depth of the active channel region. Channel parameters eventually set the threshold voltage of the FET, and thus the signal swing available in linear and digital integrated circuits. The main obstacle to ion implantation processes in this area is in the reproducible conversion of implanted impurities into active donors. As noted earlier, carrier activation in GaAs is far from complete, so that variations in the damage structure and in the starting material are reflected in run-to-run variations in the doping concentration [106]. Carrier activation is greatly improved by implantation into heated substrates. However, this can result in anomalous enhanced diffusion during the implantation, so that control of channel depth is not as tight as can normally be expected from this technique. Nevertheless, practical high-speed integrated circuits [107] as well as millimeter-wave integrated circuits (MMICs) [108] are already being successfully fabricated by ion implantation, and developments in the area are extremely rapid.

FROM:

VLSI FABRICATION PRINCIPLES

Second Edition

by: Sorab K. Ghandhi

1994

EXHIBIT A